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**TRANSMITTAL  
FORM**

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<b>TRANSMITTAL FORM</b>  (to be used for all correspondence after initial filing)	<b>Application Number</b>	10/072,931
	<b>Filing Date</b>	February 12, 2002
	<b>First Named Inventor</b>	Shunpei YAMAZAKI et al.
	<b>Group Art Unit</b>	2812
	<b>Examiner Name</b>	S. Isaac
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**ENCLOSURES (check all that apply)**

<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment / Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Response to Missing Parts/Incomplete Application <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Assignment Papers (for an Application) <input type="checkbox"/> Drawing(s) <input type="checkbox"/> Declaration and Power of Attorney <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) _____	<input type="checkbox"/> After Allowance Communication to Group <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input type="checkbox"/> Appeal Communication to Group (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Other Enclosures 1. Submission of Verified English Translation of Japanese Application No. 2001-040837 2. Verified English translation of priority Japanese Application No. 2001-040837 3. 4. 5. 6.
<b>Remarks</b> <input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge any additional fees required or credit any overpayments to Deposit Account No. 50-2280 for the above identified docket number.		

**SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT**

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<b>Date</b>	October 5, 2005

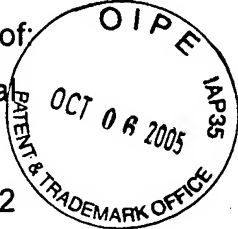
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:  
Shunpei YAMAZAKI et al  
Serial No. 10/072,931  
Filed: February 12, 2002  
For: METHOD OF MANUFACTURING A  
SEMICONDUCTOR DEVICE



) Group Art Unit: 2812  
) Examiner: S. Isaac

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**SUBMISSION OF VERIFIED ENGLISH TRANSLATION**

**OF JAPANESE APPLICATION NO. 2001-040837**

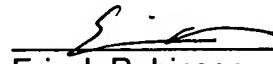
Honorable Commissioner of Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

Further to the Amendment filed August 22, 2005, a verified English translation of priority application JP 2001-040837 filed February 16, 2001 is submitted herewith. Since Chan has an earliest effective U.S. filing date of February 21, 2001, which is later than the filing date of JP '837, the Applicants respectfully submit that the rejection under § 103 should be overcome. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103 are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

  
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Shunpei YAMAZAKI et al.

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For: METHOD OF MANUFACTURING  
A SEMICONDUCTOR DEVICE



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) Examiner: S. Isaac

) Group Art Unit: 2812

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VERIFICATION OF TRANSLATION

Commissioner for Patents

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Sir:

I, Sachiko Sasayama, C/O Semiconductor Energy Laboratory Co., Ltd. 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan, a translator, herewith declare:

that I am well acquainted with both the Japanese and English Languages;

that I am the translator of the attached translation of the Japanese Patent Application No. 2001-040837 filed on February 16, 2001; and

that to the best of my knowledge and belief the followings is a true and correct translation of the Japanese Patent Application No. 2001-040837 filed on February 16, 2001.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 22<sup>nd</sup> day of September, 2005

A handwritten signature in cursive script, reading "S. Sasayama".

Name: Sachiko Sasayama



[Name of Document] Patent Application

[Number] P005530

[Filing Date] February 16, H13 (2001)

[Attention] Commissioner of the JPO, Kozo Oikawa

[International Patent Classification] H01L 21/00

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[List of Attachment]	
[Attachment]	Specification 1
[Attachment]	Drawing 1
[Attachment]	Abstract 1
[Necessity of Proof]	Necessary

[Document Name] Specification

[Title of the Invention] METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

[Scope of Claim]

[Claim 1]

A method of manufacturing a semiconductor device characterized by comprising of:

- a first step of adding a metal element to a first semiconductor film having an amorphous structure;

- a second step of crystallizing the first semiconductor film to form a first semiconductor film having a crystalline structure;

- a third step of forming a barrier layer on a surface of the first semiconductor film having a crystalline structure;

- a fourth step of forming a second semiconductor film on the barrier layer;

- a fifth step of forming a third semiconductor film comprising a rare gas element at a concentration of  $1 \times 10^{19}$  to  $1 \times 10^{22} / \text{cm}^3$  on the second semiconductor film;

- a sixth step of gettering the metal element into the third semiconductor film to remove or reduce the amount of the metal element within the first semiconductor film having a crystalline structure; and

- a seventh step of removing the second semiconductor film and the third semiconductor film.

[Claim 2]

A method of manufacturing a semiconductor device according to claim 1 characterized in that; the fifth step comprises steps of forming a semiconductor film and adding a rare gas element to the semiconductor film.

[Claim 3]

A method of manufacturing a semiconductor device according to claim 1 characterized in that; the fifth step comprises a step of forming a third semiconductor film comprising a rare gas element by using plasma CVD or reduced pressure thermal CVD.

[Claim 4]

A method of manufacturing a semiconductor device according to claim 1 characterized in that; the fifth step comprises a step of forming a third semiconductor film comprising a rare gas element by using sputtering.

[Claim 5]

A method of manufacturing a semiconductor device according to claim 3 or 4

characterized in that; the fifth step comprises a step of forming the third semiconductor film comprising a rare gas element and further comprises a step of adding a rare gas element to the third semiconductor film.

[Claim 6]

A method of manufacturing a semiconductor device according to claim 2 or 5 characterized by adding one element or a plurality of elements selected from the group consisting of O, O<sub>2</sub>, P, H, and H<sub>2</sub> in addition to the rare gas element.

[Claim 7]

A method of manufacturing a semiconductor device according to any one of claims 1 to 6 characterized in that; the third semiconductor film is a semiconductor film having an amorphous structure or a crystalline structure.

[Claim 8]

A method of manufacturing a semiconductor device characterized by comprising of:

a first step of adding a metal element to a first semiconductor film having an amorphous structure;

a second step of crystallizing the first semiconductor film to form a first semiconductor film having a crystalline structure;

a third step of forming a barrier layer on a surface of the first semiconductor film having a crystalline structure;

a fourth step of forming a second semiconductor film on the barrier layer;

a fifth step of adding a rare gas element at a concentration of  $1 \times 10^{19}$  to  $1 \times 10^{22}$  /cm<sup>3</sup> to an upper layer of the second semiconductor film;

a sixth step of gettering the metal element into the upper layer of the second semiconductor film to remove or reduce the amount of the metal element within the first semiconductor film having a crystalline structure; and

a seventh step of removing the second semiconductor film.

[Claim 9]

A method of manufacturing a semiconductor device according to claim 8, characterized by adding one element or a plurality of elements selected from the group consisting of O, O<sub>2</sub>, P, H, and H<sub>2</sub> in addition to the rare gas element of the fifth step.

[Claim 10]

A method of manufacturing a semiconductor device according to any one of claims 1 to 9 characterized in that; the second semiconductor film is a semiconductor film having an amorphous structure or a crystalline structure.

[Claim 11]

A method of manufacturing a semiconductor device according to any one of claims 1 to 10 characterized in that; the metal element is one element or a plurality of elements selected from the group consisting of Fe, Ni, Co, Ru, Rh, Pd, Os, Ir, Pt, Cu, and Au.

[Claim 12]

A method of manufacturing a semiconductor device according to any one of claims 1 to 11 characterized in that; the second step is a heat treatment process.

[Claim 13]

A method of manufacturing a semiconductor device according to any one of claims 1 to 11 characterized in that; the second step is a process of irradiating strong light to the semiconductor film having an amorphous structure.

[Claim 14]

A method of manufacturing a semiconductor device according to any one of claims 1 to 11 characterized in that; the second step is a heat treatment process and a process of irradiating strong light to the semiconductor film having an amorphous structure.

[Claim 15]

A method of manufacturing a semiconductor device according to any one of claims 1 to 14 characterized in that; the third step of forming the barrier layer is a step of oxidizing a surface of the semiconductor film having a crystalline structure by using a solution containing ozone.

[Claim 16]

A method of manufacturing a semiconductor device according to any one of claims 1 to 14 characterized in that; the third step of forming the barrier layer is a step of oxidizing a surface of the semiconductor film having a crystalline structure by irradiating ultraviolet light.

[Claim 17]

A method of manufacturing a semiconductor device according to any one of claims 1 to 16 characterized in that; the sixth step is a heat treatment process.

[Claim 18]

A method of manufacturing a semiconductor device according to any one of claims 1 to 16 characterized in that; the sixth step is a process of irradiating strong light to the semiconductor film.

[Claim 19]

A method of manufacturing a semiconductor device according to any one of claims 1 to 16 characterized in that; the sixth step is a heat treatment process and a



process of irradiating strong light to the semiconductor film.

[Claim 20]

A method of manufacturing a semiconductor device according to any one of claims 13, 14, 18 and 19 characterized in that; the strong light is light emitted from a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp.

[Claim 21]

A method of manufacturing a semiconductor device according to any one of claims 1 to 20 characterized in that; the rare gas element is one element or a plurality of elements selected from the group consisting of He, Ne, Ar, Kr, and Xe.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention pertains]

The present invention relates to a method of manufacturing a semiconductor device using a gettering technique. In particular, the present invention relates to a method of manufacturing a semiconductor device that uses a crystalline semiconductor film manufactured by adding a metal element having a catalytic action in crystallizing a semiconductor film.

[0002]

Note that, throughout this specification, the term semiconductor device indicates general devices capable of functioning by utilizing semiconductor properties. Electro-optical devices, semiconductor circuits, and electronic devices are all semiconductor devices.

[0003]

[Prior Art]

Thin film transistors (hereafter referred to as TFTs) are known as typical semiconductor elements that use a semiconductor film having a crystalline structure (hereafter referred to as crystalline semiconductor film). TFTs are in the spotlight as a technique of forming an integrated circuit on an insulating substrate such as glass, and devices such as liquid crystal display devices having integrated driver circuits are being put into practical use. In conventional techniques, crystalline semiconductor films are manufactured from an amorphous semiconductor film deposited by plasma CVD or reduced pressure CVD by using a heat treatment process or a laser annealing method (a technique in which a semiconductor film is crystallized by irradiation of laser light).

[0004]

A crystalline semiconductor film thus manufactured is an aggregate of a

plurality of crystal grains, and its crystal orientation is arranged in arbitrary directions. It is impossible to control the crystal orientation, and this consequently causes limitations in properties of the TFT. In solving this problem, Japanese Patent Application Laid-open No. Hei 7-183540 discloses a technique in which a metal element having a catalytic action with respect to semiconductor film crystallization, such as nickel, is added and a crystalline semiconductor film is then manufactured. This not only has an effect of lowering a heating temperature required for crystallization, but it also becomes possible to increase the crystal orientation arrangement to become more unidirectional. If a TFT is formed by using this type of crystalline semiconductor film, then not only does it become possible to increase the electric field effect mobility, but a subthreshold coefficient (S value) also becomes smaller, and electrical properties increase significantly.

[0005]

However, if a metal element having a catalytic action for crystallization is added, the metal element remains within the crystalline semiconductor film or on the surface of the film, and there are problems such as fluctuation in properties of elements obtained. Examples thereof include problems such as an increase in an off current in the TFT and its fluctuation between the individual elements. That is, the metal elements that have a catalytic action for crystallization exist unnecessarily after the crystalline semiconductor film is formed.

[0006]

Gettering using phosphorous is an effective and often used method for removing this type of metal element from specified regions of the crystalline semiconductor film. For example, it is possible to easily remove the metal elements from a channel forming region by performing a heat treatment process at a temperature of 450 to 700°C by adding phosphorous to a source or drain region of the TFT.

[0007]

Phosphorous is injected into the crystalline semiconductor film by an ion doping method (this indicates a method of dissociating  $\text{PH}_3$  or the like by a plasma, accelerating the ions by using an electric field, and injecting the ions into the semiconductor film; the ion doping method is basically a method in which separation of mass of ions is not performed). The concentration of phosphorous necessary for gettering is equal to or greater than  $1 \times 10^{20} / \text{cm}^3$ . Adding phosphorous by ion doping can cause a crystalline semiconductor film to take on amorphous qualities, and the increase in the phosphorous concentration hinders recrystallization during a later annealing process, thus becoming a problem. Further, the addition of a high

concentration of phosphorous causes an increase in the required amount of processing time for doping, and throughput of the doping process is decreased, thus becoming a problem.

[0008]

[Problems to be Solved by the Invention]

An object of the present invention is to reduce the number of high temperature (greater than 600°C) heat treatment processes and achieve further lower temperature (equal to or less than 600°C) processes, and to simplify the processes and to increase throughput.

[0009]

[Means for Solving the Problem]

The present invention has: a step of forming a first semiconductor film having a crystalline structure by using a metal element; a step of forming a film that becomes an etching stopper (barrier layer); a step of forming a second semiconductor film; a step of forming a third semiconductor film containing a rare gas element (gettering sites); a step of gettering the metal element to the gettering sites; and a step of removing the second semiconductor film and the third semiconductor film.

[0010]

Further, in the step of forming the third semiconductor film containing the rare gas element (gettering sites), the rare gas element may also be added to the semiconductor film after forming the semiconductor film having an amorphous structure or a crystalline structure. Ion doping or ion injection may be used as a method for adding the rare gas element. Note that film formation conditions are regulated so that film peeling does not develop.

[0011]

One element, or a plurality of elements, selected from the group consisting of H, H<sub>2</sub>, O, O<sub>2</sub> and P may also be added in addition to the rare gas element. A synergistic gettering effect can be obtained by thus adding a plurality of elements. Among the group, O and O<sub>2</sub> are particularly effective, and gettering efficiency is increased if oxygen concentration is equal to or greater than  $5 \times 10^{18} / \text{cm}^3$ , preferably in a concentration range from  $1 \times 10^{19} / \text{cm}^3$  to  $1 \times 10^{22} / \text{cm}^3$  within the second semiconductor film or the third semiconductor film as measured by SIMS analysis by the film formation conditions or the addition after film formation. Note that the rare gas element has almost no diffusion. If another element added in addition to the rare gas element diffuses easily, then it is preferable to regulate the film thickness of the second semiconductor film such that the other added element does not diffuse to the first

semiconductor film due to later heat treatment processes. Furthermore, in addition to the second semiconductor film, the barrier layer also functions to prevent diffusion of the other element.

[0012]

The step of forming the third semiconductor film containing the rare gas element (gettering sites) may also be performed by employing plasma CVD or reduced pressure thermal CVD using a raw material gas containing the rare gas element. However, the film formation conditions are regulated so that film peeling does not develop.

[0013]

Experimental results are shown below in Table 1 for measurements of an internal stress within amorphous silicon films (samples A to L) having a film thickness of 2000Å and formed by using silane gas ( $\text{SiH}_4$ , 100 sccm) as a film formation gas (flow rate) and changing the flow rate of an argon gas between 0 sccm, 100 sccm, 200 sccm, 300 sccm, 400 sccm, and 500 sccm.

[0014]

[Table 1]

Film formation conditions:  $\text{SiH}_4$  = 100, Ar = 0 to 500, 0.25 Torr, Gap 35 mm, RF power 35W (continuous oscillation)

Sample No.	Ar flow rate [sccm]	Film thickness [Å]	Stress [dyn/cm <sup>2</sup> ]	Stress direction
A	0	1935	1.12E+09	tensile
B	0	1935	1.13E+09	tensile
C	100	2022	1.68E+09	tensile
D	100	2022	1.31E+09	tensile
E	200	1992	1.18E+09	tensile
F	200	1992	1.18E+09	tensile
G	300	1973	1.55E+09	tensile
H	300	1973	1.36E+09	tensile
I	400	1917	1.34E+09	tensile
J	400	1917	1.37E+09	tensile
K	500	1945	1.31E+09	tensile
L	500	1945	1.34E+09	tensile

[0015]

Further, a graph of Table 1 is shown in FIG. 16, and a comparative example of an amorphous silicon film with pulse oscillation is also shown. A compressive stress

(approximately  $9.7 \times 10^9$  dynes/cm<sup>2</sup>) is shown for the amorphous silicon film formed by using RF pulse oscillation, and therefore there is a concern that film peeling will develop. Consequently, it is preferable to form films by using RF continuous oscillation at the conditions showing tensile stresses ( $1.12$  to  $1.68 \times 10^9$  dynes/cm<sup>2</sup>) of Table 1. The second semiconductor film that does not contain the rare gas element may be formed by conditions of the sample A or B, and it is preferable to form the third semiconductor film that contains the rare gas element by using one set of conditions from among those of samples C to L.

[0016]

Note that the amorphous silicon films used in the aforementioned experiment and deposited by plasma CVD (PCVD apparatus) are formed at an RF power of 35 W and a film formation pressure of 0.25 Torr.

[0017]

In general, an internal stress is either a tensile stress or a compressive stress. When a thin film tries to contract with respect to a substrate, the substrate pulls in a direction so as to prevent the contraction, the substrate changes shape with the thin film inside. This is referred to as a tensile stress. If the thin film tries to expand, then the substrate is pushed back and formed with the thin film outside. This is referred to as a compressive stress.

[0018]

The third semiconductor film containing the rare gas element may also be formed by sputtering. The rare gas element may additionally be added at the film formation stage after obtaining the third semiconductor film containing the rare gas to increase the gettering efficiency.

[0019]

One structure of the present invention disclosed by this specification is a method of manufacturing a semiconductor device characterized by composing of:

- a first step of adding a metal element to a first semiconductor film having an amorphous structure;

- a second step of crystallizing the first semiconductor film, forming a first semiconductor film having a crystalline structure;

- a third step of forming a barrier layer on a surface of the first semiconductor film having a crystalline structure;

- a fourth step of forming a second semiconductor film on the barrier layer;

- a fifth step of forming a third semiconductor film, containing a rare gas element at a concentration of  $1 \times 10^{19}$  to  $1 \times 10^{22}$  /cm<sup>3</sup>, on the second semiconductor film;

a sixth step of gettering the metal element into the third semiconductor film, removing or reducing the amount of the metal element within the first semiconductor film having a crystalline structure; and

a seventh step of removing the second semiconductor film and the third semiconductor film.

[0020]

In the above structure, the fifth step may be made into: a step of forming a semiconductor film and a step of adding a rare gas element to the semiconductor film; or a step of forming a third semiconductor film containing a rare gas element by using plasma CVD or reduced pressure thermal CVD; or into a step of forming a third semiconductor film containing a rare gas element by using sputtering.

[0021]

Further, if the rare gas element is added in the above structure, it is preferable to also add one element or a plurality of elements selected from the group consisting of O, O<sub>2</sub>, P, H, and H<sub>2</sub> at the same step or sequentially in addition to the rare gas element.

[0022]

In the above structure, it is characterized in that the third semiconductor film is a single layer, or a lamination structure, of a semiconductor film having an amorphous structure or a crystalline structure and formed by plasma CVD, reduced pressure CVD, or sputtering. Furthermore, it is preferable that the third semiconductor film have a tensile stress.

[0023]

The present invention is not limited to the above structure, and gettering sites may also be formed by adding a rare gas element only on the upper layer of the second semiconductor film, without forming the third semiconductor film.

[0024]

A second structure of the present invention is a method of manufacturing a semiconductor device characterized by comprising of:

a first step of adding a metal element to a first semiconductor film having an amorphous structure;

a second step of crystallizing the first semiconductor film, forming a first semiconductor film having a crystalline structure;

a third step of forming a barrier layer on a surface of the first semiconductor film having a crystalline structure;

a fourth step of forming a second semiconductor film on the barrier layer;

a fifth step of adding a rare gas element at a concentration of  $1 \times 10^{19}$  to  $1 \times 10^{22}$

/cm<sup>3</sup> to an upper layer of the second semiconductor film;

a sixth step of gettering the metal element into the upper layer of the second semiconductor film, removing or reducing the amount of the metal element within the first semiconductor film having a crystalline structure; and

a seventh step of removing the second semiconductor film.

[0025]

It is preferable to also add one element, or a plurality of elements selected from the group consisting of O, O<sub>2</sub>, P, H, and H<sub>2</sub> at the same step or sequentially in addition to the rare gas element in the fifth step of the above structure.

[0026]

Furthermore, in both of the above structures, it is characterized in that the second semiconductor film is a single layer or a lamination layer of a semiconductor film having an amorphous structure or a crystalline structure and formed by plasma CVD, reduced pressure thermal CVD, or sputtering. Furthermore, it is preferable that the second semiconductor film have a tensile stress.

[0027]

Further, it is characterized in that the metal element in each of the above structures is an element or a plurality of elements selected from the group consisting of Fe, Ni, Co, Ru, Rh, Pd, Os, Ir, Pt, Cu, and Au.

[0028]

Further, it is characterized in that the second step in each of the above structures is a one process or a combination of processes, selected from a heat treatment process, a process of irradiating strong light, and a process of irradiating laser light (excimer laser light having a wavelength equal to or less than 400 nm, or the second harmonic or third harmonic of a YAG laser).

[0029]

Further, the third step of forming the barrier layer in each of the above structures may be a step of oxidizing a surface of the semiconductor film having a crystalline structure by using a solution containing ozone, or a step of oxidizing the surface of the semiconductor film having a crystalline structure by irradiating ultraviolet light under an oxygen atmosphere.

[0030]

Further, it is characterized in that the sixth step in each of the above structures is a heat treatment process, a process of irradiating strong light to the semiconductor film having an amorphous structure, or a heat treatment process and a process of irradiating strong light to the semiconductor film having an amorphous structure.

[0031]

Further, in each of the above structures, if strong light is irradiated, then light emitted from a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp is used.

[0032]

Further, it is characterized in that the rare gas element in each of the above structures is one element or a plurality of elements, selected from the group consisting of He, Ne, Ar, Kr, and Xe.

[0033]

[Embodiment Modes of the Invention]

Embodiment modes of the invention are explained below.

[00034]

One aspect of the present invention has a process of forming a barrier layer and a semiconductor film on a crystalline semiconductor film, a process of forming a semiconductor film containing a rare gas element (gettering sites) on the upper side of crystalline semiconductor film, and a process of performing a heat treatment process. A metal contained in the crystalline semiconductor film moves due to the heat treatment process, and passes through the barrier layer and the semiconductor film (the semiconductor film that does not contain the ion of the rare gas element), and is captured in the gettering sites (the semiconductor film containing the ion of the rare gas element). The metal element is thus removed from or its amount is reduced in the crystalline semiconductor film. Note that strong light may also be irradiated as a substitute for the heat treatment process, and that the irradiation of strong light may be performed at the same time as the heat treatment process.

[0035]

(Embodiment mode 1)

A typical manufacturing process is simply described below using FIG. 1.

[0036]

Reference numeral 100 in FIG. 1A denotes a substrate having an insulating surface, reference numeral 101 denotes a base insulating film, and reference numeral 102 denotes a semiconductor film having an amorphous structure.

[0037]

First, the base insulating film 101 made from an insulating film such as a silicon oxide film, a silicon nitride film, or a silicon oxynitride film is formed on the substrate 100 as a blocking layer. A two layers structure (a silicon oxynitride film having a film thickness of 50 nm and a silicon oxynitride film having a film thickness of



100 nm) is used here as the base insulating film 101, but a single layer film or a structure in which two or more layers are laminated may also be used. Note that the base insulating film may not necessarily be formed if it is unnecessary to form a blocking layer.

[0038]

Next, the semiconductor film 102 having an amorphous structure on the base insulating film is crystallized by using a known means, forming a semiconductor film 104 having a crystalline structure. (See FIG. 1B.)

[0039]

In the present invention, the semiconductor film having a crystalline structure may be formed by adding a metal element to the semiconductor film 102 having an amorphous structure, which has been obtained by plasma CVD, reduced pressure thermal CVD, or sputtering, and next performing crystallization by a heat treatment process or irradiation of strong light. An amorphous silicon film is formed here, and a solution containing nickel is applied to the amorphous silicon film, forming a nickel containing layer 103.

[0040]

After the crystallization, the segregated metal element may be removed or reduced in its amount by using an etchant containing hydrofluoric acid, for example dilute hydrofluoric acid or FPM (a liquid mixture of hydrofluoric acid, hydrogen peroxide, and pure water). Further, it is preferable to irradiate strong light and perform leveling of the surface if the surface is etched using an etchant containing hydrofluoric acid.

[0041]

Irradiation of laser light or strong light may also be performed after the crystallization in order to further improve the crystallization. The segregated metal element may be removed or reduced in its amount by using an etchant containing hydrofluoric acid after the irradiation of laser light or strong light in order to improve the crystallization. In addition, strong light may also be irradiated for surface leveling.

[0042]

Note that it is preferable that the semiconductor film 104 having a crystalline structure be formed such that oxygen concentration within the semiconductor film 104 is less than or equal to  $5 \times 10^{18} / \text{cm}^3$  (SIMS analysis).

[0043]

Next, a barrier layer 105 having silicon as its main constituent is formed on the semiconductor film 104 having a crystalline structure. Note that the barrier layer 105

may be extremely thin, and may also be a natural oxidation film. In addition, ozone may be generated by irradiating ultraviolet light under an atmosphere containing oxygen, forming an oxide film. Furthermore, an oxide film that is oxidized by using a solution containing ozone that is used in surface processing known as hydro washing, performed for removing carbon, namely organic matter, may also be used as the barrier layer 105. The barrier layer 105 is mainly used as an etching stopper. Channel doping may also be performed after forming the barrier layer 105, and then strong light may be irradiated to perform activation.

[0044]

A second semiconductor film 106 is then formed on the barrier layer 105. The second semiconductor film 106 may be a semiconductor film having an amorphous structure, and it may also be a semiconductor film having a crystalline structure. The film thickness of the second semiconductor film 106 is set from 5 to 50 nm, preferably between 10 and 20 nm. It is preferable to include oxygen in the second semiconductor film 106 (at a concentration measured by SIMS analysis equal to or greater than  $5 \times 10^{18} / \text{cm}^3$ , preferably equal to or greater than  $1 \times 10^{19} / \text{cm}^3$ ) to increase gettering efficiency.

[0045]

A third semiconductor film 107 containing a rare gas element (gettering sites) is formed on the second semiconductor film 106. The third semiconductor film 107 may be formed by plasma CVD, reduced pressure thermal CVD, or by sputtering, and may have an amorphous structure or a crystalline structure. The third semiconductor film may be a semiconductor film containing a rare gas element at a film formation stage, or a rare gas element may be added after formation of a semiconductor film not containing a rare gas element. An example is shown in FIG. 1 in which the third semiconductor film 107 is formed containing a rare gas element at the film formation stage, and then the rare gas element is additionally added selectively, forming a third semiconductor film 108. Furthermore, the second semiconductor film and the third semiconductor film may be formed in succession without exposure to the atmosphere. The sum of the film thickness of the second semiconductor film and the film thickness of the third semiconductor film may be from 30 to 200 nm, for example 50 nm.

[0046]

A gap is opened between the first semiconductor film 104 and the third semiconductor film 108 (gettering sites) by the second semiconductor film 106 with the present invention. There is a tendency for the metal elements to easily gather near the boundaries of the gettering sites during gettering, and therefore it is preferable to keep the boundaries of the gettering sites far away from the first semiconductor film 104 to

increase gettering efficiency by using the second semiconductor film 106 as in the present invention. In addition, the second semiconductor film 106 also is effective in blocking impurity elements contained in the gettering sites from diffusing during the gettering process and reaching an interface with the first semiconductor film. The second semiconductor film 106 also has a protective effect so that damage is not imparted to the first semiconductor film if rare gas elements are added.

[0047]

Gettering is performed next. A heat treatment process is performed within a nitrogen atmosphere at 450 to 800°C for 1 to 24 hours as a process for performing gettering, for example at 550°C for 14 hours. Furthermore, strong light may also be irradiated as a substitute to a heat treatment process. Strong light may also be irradiated in addition to heat treatment. Nickel moves in the direction of an arrow in FIG. 1E due to the gettering, and the metal element contained in the semiconductor film 104 covered with the barrier layer 105 is removed, or reduced in concentration. Sufficient gettering is performed here so that nickel is not segregated in the first semiconductor film 104, but moves to the third semiconductor film 108 so that almost no nickel exists in the first semiconductor film 104. That is, the nickel concentration within the film is made less than or equal to  $1 \times 10^{18} / \text{cm}^3$ , preferably less than or equal to  $1 \times 10^{17} / \text{cm}^3$ .

[0048]

Next, only the semiconductor films denoted by reference numerals 106 and 108 are selectively removed, with the barrier layer 105 acting as an etching stopper, and a semiconductor layer 109 is formed having a desired shape by using a known patterning technique on the semiconductor film 104.

[0049]

After then cleaning the surface of the semiconductor layer using an etchant containing hydrofluoric acid, an insulating film having silicon as its main constituent is formed, becoming a gate insulating film 110. It is preferable to perform the surface cleaning and the formation of the gate insulating film in succession, without exposure to the atmosphere.

[0050]

A gate electrode 111 is formed after cleaning the surface of the gate insulating film, and an impurity element that imparts n-type conductivity to a semiconductor (such as P or As) is suitably added, forming a source region 112 and a drain region 113. Phosphorous is used here. A heat treatment process, irradiation of strong light, or irradiation of laser light is then performed after the addition process in order to activate

the impurity element. Furthermore, plasma damage to the gate insulating film, and plasma damage to the interface between the gate insulating film and the semiconductor layer can be restored at the same time as activation is performed. In particular, it is extremely effective to perform activation of the impurity element by irradiating the second harmonic of a YAG laser from the top surface, or from the rear surface, in an atmosphere from a room temperature to 300°C. The use of a YAG laser is a preferable activation means because of its low maintenance.

[0051]

Subsequent steps include: forming an interlayer insulating film 115, performing hydrogenation, forming contact holes reaching the source region and the drain region, and forming a source electrode 116 and a drain electrode 117, thereby completing a TFT.

[0052]

The TFT thus obtained has, at least, nickel elements removed from a channel forming region 114, and also does not contain rare gas elements.

[0053]

The present invention is not limited to the structure shown in FIG. 1. A low concentration drain (LDD, lightly doped drain) structure having an LDD region between the channel forming region and the drain region (or the source region) may also be used if necessary. This structure is one in which a region having a low concentration of an added impurity element is formed between the channel forming region and the source region or the drain region formed by adding a high concentration impurity element, and this region is referred to as an LDD region. In addition, a GOLD (gate-drain overlapped LDD) structure in which the LDD region overlaps with the gate electrode with the gate insulating film interposed therebetween may also be used.

[0054]

Further, although an n-channel TFT is used for the explanation here, it is of course also possible to form a p-channel TFT by using an impurity element that imparts p-type conductivity to a semiconductor as a substitute for the impurity element that imparts n-type conductivity to a semiconductor.

[0055]

An example of a top gate TFT is explained here, but it is possible to apply the present invention regardless of the TFT structure. For example, it is possible to apply the present invention to a bottom gate TFT (reverse stagger type) and to a forward stagger TFT.

[0056]

(Embodiment mode 2)

Gettering sites may also be formed by adding a rare gas element to only the upper layer of the second semiconductor film, without forming the third semiconductor film, shown in Embodiment mode 1. An example of this is explained here using FIG. 2.

[0057]

Manufacturing up through the formation of a barrier layer 205 is similar to that of Embodiment mode 1. A base insulating film 201 is formed on a substrate 200, and the barrier layer 205 is formed after forming a semiconductor film 204 having a crystalline structure, all in accordance with Embodiment mode 1. Crystallization is also performed here using nickel, as in Embodiment mode 1. Note that FIG. 2A corresponds to FIG. 1A, and that FIG. 2B corresponds to FIG. 1B.

[0058]

A second semiconductor film 206 is formed next on the barrier layer 205. (See FIG. 2C.) The second semiconductor film 206 does not contain a rare gas element. A semiconductor film having an amorphous structure may be formed, and a semiconductor film having a crystalline structure may also be formed. It is preferable to include oxygen in the second semiconductor film 206 (at a concentration measured by SIMS analysis equal to or greater than  $5 \times 10^{18} / \text{cm}^3$ , preferably equal to or greater than  $1 \times 10^{19} / \text{cm}^3$ ) to increase gettering efficiency.

[0059]

A rare gas element is then added to an upper layer of the second semiconductor film 206. A region to which the rare gas element is added is denoted by reference numeral 207, as shown in FIG. 2D. The region 207 becomes gettering sites.

[0060]

Gettering is performed next. A heat treatment process is performed within a nitrogen atmosphere at 450 to 800°C for 1 to 24 hours as a process for performing gettering, for example at 550°C for 14 hours. Strong light may also be irradiated as a substitute to the heat treatment process. Strong light may also be irradiated in addition to the heat treatment process. Nickel moves in the direction of an arrow in FIG. 2E due to the gettering, and the metal element contained in the semiconductor film 204 covered with the barrier layer 205 is removed, or reduced in concentration. Sufficient gettering is performed here so that nickel is not segregated in the first semiconductor film 204, but moves to the upper layer 207 of the second semiconductor film, and almost no nickel exists in the first semiconductor film 204.

[0061]

Next, only the semiconductor films denoted by reference numerals 206 and 207 are selectively removed, with the barrier layer 205 acting as an etching stopper, and a semiconductor layer 208 is formed having a desired shape by using a known patterning technique on the semiconductor film 204.

[0062]

Subsequent process steps are in accordance with Embodiment mode 1, and a gate insulating film 209 and a gate electrode 210 are formed. After forming a source region 211 and a drain region 212 by performing addition of an impurity element that imparts n-type conductivity to a semiconductor, an interlayer insulating film 214 is formed. Hydrogenation is then performed, and contact holes for reaching the source region and the drain region are formed. A TFT is completed after forming a source electrode 215 and a drain electrode 216.

[0063]

The TFT thus obtained also has, at least, nickel elements removed from a channel forming region 213, and also does not contain rare gas elements in the channel forming region 213.

[0064]

An additionally detailed explanation of the present invention having the above structures is made using embodiments shown below.

[0065]

(Embodiments)

[Embodiment 1]

Here, a method of manufacturing a pixel portion and driver circuit TFTs (an n-channel TFT and a p-channel TFT) formed in the periphery of the pixel portion at the same time and on the same substrate is explained using FIGS. 3 to 5.

[0066]

First, a substrate 200 made from a glass such as barium borosilicate glass or aluminum borosilicate glass, typically Corning Corp. #7059 glass or #1737 glass, is used in the present embodiment. Note that, provided that the substrate has transparency to light, a quartz substrate may also be used as the substrate 300. Further, a plastic substrate having resistance to heat that is able to withstand the processing temperatures of the present embodiment may also be used.

[0067]

Next, a base film 301 made from an insulating film such as a silicon oxide film, a silicon nitride film, or a silicon oxynitride film is formed on the substrate 300. A two layer structure is used as the base film 301 in the present embodiment, but a single layer

insulating film or one having a lamination structure with more than two such layers may also be used. A silicon oxynitride film 301a deposited using plasma CVD and with  $\text{SiH}_4$ ,  $\text{NH}_3$ , and  $\text{N}_2\text{O}$  as reaction gasses is formed having a film thickness of 10 to 200 nm (preferably between 50 and 100 nm) as a first layer of the base film 301. A silicon oxynitride film 301a having a film thickness of 50 nm (composition ratio: Si = 32%, O = 27%, N = 24%, and H = 17%) is formed in the present embodiment. Next, a silicon oxynitride film 301b deposited using plasma CVD and with  $\text{SiH}_4$  and  $\text{N}_2\text{O}$  as reaction gasses is formed having a film thickness of 50 to 200 nm (preferably between 100 and 150 nm) as a second layer of the base film 301. A silicon oxynitride film 301b having a film thickness of 100 nm (composition ratio: Si = 32%, O = 59%, N = 7%, and H = 2%) is formed in the present embodiment.

[0068]

Semiconductor layers 302 to 306 are formed next on the base film. After forming a semiconductor film having an amorphous structure by a known means (such as sputtering, LPCVD, or plasma CVD), a known crystallization process (such as laser crystallization, thermal crystallization, or thermal crystallization using a catalyst such as nickel) is performed. The crystalline semiconductor film obtained is then patterned into a desired shape to thereby obtain each of the semiconductor layers 302 to 306. The semiconductor layers 302 to 306 are formed having a thickness of 25 to 80 nm (preferably from 30 to 60 nm). There are no limitations placed on the crystalline semiconductor film material, but it is preferable to use silicon or a silicon germanium alloy ( $\text{Si}_x\text{Ge}_{1-x}$ , where  $x = 0.0001$  to  $0.02$ ). For example, a silicon germanium film is formed containing from 0.02 to 2 atom% of germanium with respect to silicon.

[0069]

After forming an amorphous silicon film having a thickness of 55 nm using plasma CVD, a solution containing nickel is maintained on the amorphous silicon film in the present embodiment. Thermal crystallization (at  $550^\circ\text{C}$  for 4 hours) is performed after performing dehydrogenation (at  $500^\circ\text{C}$  for 1 hour) of the amorphous silicon film. Laser annealing is then performed in order to further improve crystallization, and a crystalline silicon film is formed. Then, in accordance with Embodiment mode 1, an extremely thin oxide film is formed on the surface by using a solution containing ozone. A second semiconductor film containing oxygen (at a concentration measured by SIMS analysis equal to or greater than  $5 \times 10^{18} / \text{cm}^3$ , preferably equal to or greater than  $1 \times 10^{19} / \text{cm}^3$ ), and a third semiconductor film containing a rare gas element are formed on the oxide film. Gettering is then performed in accordance with Embodiment mode 1 by performing a heat treatment

process, after which the second semiconductor film and the third semiconductor film, using the oxide film as etching stoppers, are removed. The crystalline silicon film is patterned, and the oxide film is removed. The semiconductor layers 302 to 306 made from the crystalline silicon film, in which the nickel concentration is equal to or less than  $1 \times 10^{18} / \text{cm}^3$ , preferably equal to or less than  $1 \times 10^{17} / \text{cm}^3$ , are thus formed. A state after patterning of the semiconductor layers 302 to 306 is completed corresponds to FIG. 1F in Embodiment mode 1. Note that after forming the oxide film, doping (also referred to as channel doping) of a very small amount of an impurity element (boron or phosphorous) in order to control the TFT threshold value may also be performed appropriately.

[0070]

Cleaning of the surface of the semiconductor layers 302 to 306 is then performed using a hydrofluoric acid etchant such as buffered hydrofluoric acid. An insulating film 307 having silicon as its main constituent is formed next by plasma CVD or sputtering to a thickness of 40 to 150 nm. A 115 nm thick silicon oxynitride film (composition ratio: Si = 32%, O = 59%, N = 7%, and H = 2%) is formed by plasma CVD in the present embodiment. The insulating film, which becomes a gate insulating film, is of course not limited to a silicon oxynitride film. Other insulating films containing silicon may also be used, as single layers or as lamination layer structures.

[0071]

Next, as shown in FIG. 3A, a first conductive film 308 having a film thickness of 20 to 100 nm, and a second conductive film 309 having a film thickness of 100 to 400 nm are formed as laminated on the gate insulating film 307. The first conductive film 308 is formed from a TaN film having a film thickness of 30 nm, and the second conductive film 309 is formed to be laminated from a W film having a film thickness of 370 nm in the present embodiment. The TaN film is formed by sputtering. A Ta target is used, and sputtering is performed in an atmosphere containing nitrogen. Furthermore, the W film is formed by sputtering using a W target. In addition, the W film can also be formed by thermal CVD using tungsten hexafluoride ( $\text{WF}_6$ ).

[0072]

Note that although the first conductive film 308 is TaN, and the second conductive film 309 is W in the present embodiment, there are no particular limitations placed on these films. Both films may be formed having a single layer or a lamination layer, and from an element selected from the group consisting of Ta, W, Ti, Mo, Al, Cu, Cr, and Nd, or from an alloy material or compound material having one of the aforementioned elements as its main constituent. Further, a semiconductor film,



typically a polycrystalline silicon film in which an impurity element such as phosphorous is doped, may also be used. An AgPdCu alloy may also be used. In addition, the following may also be used: forming the first conductive film by a tantalum (Ta) film and combining it with the second conductive film formed from a W film; forming the first conductive film by a titanium nitride (TiN) film and combining it with the second conductive film formed from a W film; forming the first conductive film by a tantalum nitride (TaN) film and combining it with the second conductive film formed from an Al film; and forming the first conductive film from a tantalum nitride (TaN) film and combining it with the second conductive film formed by a Cu film.

[0073]

Masks 310 to 315 are formed next from resist using a photolithography method, and a first etching process is performed in order to form electrodes and wirings. The first etching process is performed under first and second etching conditions. An ICP (Inductively Coupled Plasma) etching method is used in the present embodiment for the first etching condition. A gas mixture of  $\text{CF}_4$ ,  $\text{Cl}_2$ , and  $\text{O}_2$  is used as an etching gas, the gas flow rates are set to 25 / 25 / 10 sccm respectively, a plasma is generated by applying a 500 W RF electric power (13.56 MHz) to a coil shape electrode at a pressure of 1 Pa, and etching is performed. Note that a chlorine gas, typically a gas such as  $\text{Cl}_2$ ,  $\text{BCl}_3$ ,  $\text{SiCl}_4$  or  $\text{CCl}_4$ , a hydrofluoride gas, typically a gas such as  $\text{CF}_4$ ,  $\text{SF}_6$ ,  $\text{NF}_3$ , or  $\text{O}_2$  can also be used as the etching gas appropriately. A Matsushita Electric Inc. Dry etching apparatus (model E645-□ICP) using an ICP is employed. A 150 W RF electric power (13.56 MHz) is also applied to the substrate side (sample stage), thereby effectively applying a negative self-bias. The W film is etched under the first etching conditions, and the edge portion of the first conductive layer is made into a tapered shape. The etching speed of W is 200.39 nm/ min under the first etching conditions, and the etching speed of TaN is 80.32 nm/ min, resulting in a selection ratio of W with respect to TaN of approximately 2.5. Further, the taper angle of W becomes approximately  $26^\circ$  under the first etching conditions.

[0074]

Thereafter, the etching conditions are changed to second etching conditions without removing the resist masks 310 to 315. A gas mixture of  $\text{CF}_4$  and  $\text{Cl}_2$  is used as an etching gas, the gas flow rates are set to 30 / 30 sccm respectively, a plasma is generated by applying a 500 W RF electric power (13.56 MHz) to a coil shape electrode at a pressure of 1 Pa, and etching is performed for approximately 30 seconds. A 20 W RF electric power (13.56 MHz) is also applied to the substrate side (sample stage), thereby effectively applying a negative self-bias. The W film and the TaN film are

both etched at a rate on the same order by the second etching conditions using the  $\text{CF}_4$  and  $\text{Cl}_2$  gas mixture. The etching speed is 58.97 nm/min with respect to W, and the etching speed is 66.43 nm/min with respect to TaN under the second etching conditions. Note that in order for etching to be performed such that no residue remains on the gate insulating film, the etching time may be increased at a rate on the order of 10 to 20%.

[0075]

Edge portions of the first conductive layer and the second conductive layer are made into a tapered shape due to the effect of a bias voltage applied to the substrate side under the above first etching conditions by using a suitable resist mask shape. The angle of the tapered portions is from 15 to 45°.

[0076]

First shape conductive layers 316 to 321 (first conductive layers 316a to 321a, and second conductive layers 316b to 321b) are thus formed from the first conductive layers and the second conductive layers by the first etching process. Although not shown in the figures, a region of the insulating film 307, that becomes a gate insulating film, which is not covered with the first shape conductive layers 316 to 321 is etched on the order of 10 to 20 nm, forming a thinner region.

[0077]

Following the first etching process, a second etching process is performed next in the present embodiment without removing the resist masks. A mixture of  $\text{SF}_6$ ,  $\text{Cl}_2$ , and  $\text{O}_2$  is used as the etching gas, the gas flow rates are set to 24 / 12 / 24 sccm respectively, a plasma is generated by applying a 700 W RF electric power (13.56 MHz) to a coil shape electrode at a pressure of 1.3 Pa, and etching is performed for approximately 25 seconds. A 10 W RF electric power (13.56 MHz) is also applied to the substrate side (sample stage), thereby effectively applying a negative self-bias. The etching speed of W is 227.3 nm/min, and the etching speed of TaN is 32.1 nm/min under the second etching conditions, resulting in a selection ratio of W with respect to TaN of 7.1. The etching speed with respect to SiON, the insulating film 307, is 33.7 nm/min, giving a selection ratio of W with respect to TaN of 6.83. Film reduction can be suppressed when using  $\text{SF}_6$  as an etching gas because the selection ratio with respect to the insulating film 307 is high. Further, reliability increases the larger the width of the tapered portion in the channel length direction becomes in the driver circuit TFTs, and therefore it is effective to perform dry etching using an etching gas containing  $\text{SF}_6$  in forming the tapered portion.

[0078]

The taper angle of W becomes 70° due to the second etching process. Second

conductive layers 322b to 327b are formed by the second etching process. The first conductive layer is almost not etched, however, and first conductive layers 322a to 327a are formed. It is also possible to use  $\text{CF}_4$ ,  $\text{Cl}_2$ , and  $\text{O}_2$  as etching gasses in the second etching process.

[0079]

Next, a first doping process is performed after the masks comprising resist are removed, and the state of FIG. 3C is obtained. The first conductive layers 322a to 327a are used as masks with respect to an impurity element, and doping is performed so that the impurity element is not added to the semiconductor layer below the tapered portion of the first conductive layers. P (Phosphorous) is used as the impurity element in the present embodiment, and plasma doping is performed using phosphine ( $\text{PH}_3$ ) 5 % hydrogen dilution gas at a gas flow rate of 30 sccm. A low concentration impurity regions ( $\text{n}^-$  regions) 328 overlapping with the first conductive layer are thus formed in a self-aligned manner. The concentration of phosphorous (P) added to the low concentration impurity regions 328 is from  $1 \times 10^{17}$  to  $1 \times 10^{19} / \text{cm}^3$ .

[0080]

The first doping process may also be performed such that the impurity element is added to the semiconductor layer below the tapered portion of the first conductive layer. A concentration gradient develops in this case in accordance with the film thickness of the tapered portion of the first conductive layer.

[0081]

Next, a second doping process is performed after forming masks 329 and 330 comprising resist, and an impurity element which imparts n-type conductivity is added to the semiconductor layers (FIG. 4A). Note that the semiconductor layer which becomes an active layer of the p-channel TFT is covered with the masks 329 and 330. The doping process may be performed by an ion doping method or an ion implantation. Phosphorous is used here as the impurity element which imparts n-type conductivity, and is added using an ion doping method with phosphine ( $\text{PH}_3$ ) 5 % hydrogen dilution gas.

[0082]

The conductive layer 323 becomes a mask with respect to phosphorous in the semiconductor layer 303 which becomes an n-channel TFT of a logic circuit portion later, and high concentration impurity regions ( $\text{n}^+$  regions) 343 and 344 are formed in a self-aligned manner by the second doping process. Further, the impurity element is also added below the tapered portion during the second doping process; thus, low concentration impurity regions ( $\text{n}^-$  regions) 333 and 334 are formed. The n-channel

TFT of a logic circuit portion formed later is only provided with regions which overlap with a gate electrode (GOLD regions). Note that in the low concentration impurity regions ( $n^-$  regions) 333 and 334, the impurity concentration (P concentration) is gradually decreased toward the inside from the edge portion of the tapered portion of the first conductive layer in the semiconductor layer overlapping with the tapered portion of the first conductive layer.

[0083]

By the second doping process, high concentration impurity regions 345 and 346 are formed in regions not covered with mask 331 and low concentration impurity regions ( $n^-$  regions) 335 and 336 are formed in regions covered with the mask 331 in the semiconductor layer 305 which later becomes an n-channel TFT of a sampling circuit portion. Consequently the n-channel TFT of the sampling circuit portion is only provided with low concentration impurity regions (LDD regions) which do not overlap with a gate electrode.

[0084]

In addition, by the second doping process, high concentration impurity regions 347 to 350 are formed in regions not covered with the mask 332 and low concentration impurity regions ( $n^-$  regions) 337 to 340 are formed in regions covered with the mask 332 in the semiconductor layer 306 which later becomes an n-channel TFT of a pixel portion. Therefore the n-channel TFT of the pixel portion is only provided with low concentration impurity regions (LDD regions) which do not overlap with a gate electrode. Furthermore, a high concentration impurity region 350 is formed in a self-aligned manner in a region which later becomes a capacitor portion of the pixel portion, and low concentration impurity regions ( $n^-$  regions) 341 and 342 are formed below the tapered portion.

[0085]

The impurity element which imparts n-type conductivity is added to the high concentration impurity regions 343 to 350 with a concentration range from  $3 \times 10^{19}$  to  $1 \times 10^{21} / \text{cm}^3$  by the second doping process.

[0086]

A rare gas element may also be added before or after the second doping process, and in this case, additional gettering can be performed in a heat treatment process later. In addition, in this case, it is preferable to use a mask formed so that the rare gas element is added to the edge portions of all of the semiconductor layers in the second doping process.

[0087]

Next, after the masks 329 to 332 are removed, the semiconductor layers which later become the active layers of the n-channel TFT are covered with masks 351 to 353, and then a third doping process is performed (FIG. 4B). A p-type impurity element is added through the tapered portions, and regions containing the p-type impurity element at a low concentration (regions overlapping with the gate electrodes (GOLD regions) 354b to 357b) are formed. Regions 354a to 357a containing the n-type impurity element at a low concentration and containing the p-type impurity element at a high concentration are formed by the third doping process. Although a low concentration of phosphorous is contained in the regions 354a to 357a, since the doping process is performed such that the concentration of boron becomes  $6 \times 10^{19}$  to  $6 \times 10^{20} / \text{cm}^3$ , these regions are used as source regions or drain regions of p-channel TFTs without any problems.

[0088]

Although the first doping process, the second doping process, and the third doping process are performed in order in the present embodiment, it is not limited in particular. The order of the process may be freely changed.

[0089]

Next, the masks comprising resist 351 to 353 are removed, and a first interlayer insulating film 358 is formed. The first interlayer insulating film 358 of thickness 10 to 200 nm is formed with an insulating film containing silicon by using a plasma CVD method or a sputtering method.

[0090]

Subsequently, a process of activating the impurity elements added to each of the semiconductor layers is performed, as shown in FIG. 4C. The activation process is performed by emitting a YAG laser or an excimer laser from the back side of the substrate. Activation of the impurity regions overlapping with the gate electrode with the insulating film interposed therebetween can be performed by emitting from the back side.

[0091]

Although an example of forming the first interlayer insulating film before performing the above activation is shown in the present embodiment, the process of forming the first interlayer insulating film may also be performed after performing the above activation.

[0092]

Next, a second interlayer insulating film 359 comprising a silicon nitride film is formed, and a heat treatment process (heat treatment for 1 to 12 hours at 300 to 550 °C)

is performed, thereby the process of hydrogenating the semiconductor layers is performed. A heat treatment process is performed for 1 hour at 410 °C under a nitrogen atmosphere in the present embodiment. This process is the process of terminating dangling bonds in the semiconductor layers by hydrogen contained in the second interlayer insulating film 359. The semiconductor layers can be hydrogenated whether or not the first interlayer insulating film exists. Plasma hydrogenation (in which hydrogen excited by a plasma is used) may also be performed as another means for the hydrogenation.

[0093]

Next, a third interlayer insulating film 360 comprising an organic insulating material is formed on the second interlayer insulating film 359. An acrylic resin film having a film thickness of 1.6  $\mu\text{m}$  is formed in the present embodiment. Patterning is then performed in order to form contact holes which reach respective high concentration impurity region. A plurality of etching processes is performed in the present embodiment. In the present embodiment, after etching the third interlayer insulating film with the second interlayer insulating film used as an etching stopper, the second interlayer insulating film is etched with the first interlayer insulating film used as an etching stopper, then the first interlayer insulating film is etched.

[0094]

Electrodes 361 to 369 which are electrically connected to the respective high concentration impurity region and a pixel electrode 370 which is electrically connected to the high concentration impurity region 349 are formed. A material having superior reflectivity, such as a film containing Al or Ag as its main component or a laminated film of such films, is used as a material of the electrodes and the pixel electrode.

[0095]

A driver circuit 401 having: a logic circuit portion 403 composed of an n-channel TFT 406 and a p-channel TFT 405, and a sampling circuit portion 404 composed of an n-channel TFT 408 and a p-channel TFT 407; and a pixel portion 402 having a pixel TFT composed of an n-channel TFT 409 and a storage capacitor 410 can be formed on the same substrate as described above (FIG. 5).

[0096]

Note that the n-channel TFT 409 uses a structure having two channel forming regions between a source region and a drain region (double gate structure) in the present embodiment. However, the present embodiment is not limited to the double gate structure, and a single gate structure in which one channel forming region is formed and a triple gate structure in which three channel forming regions are formed may also be

used.

[0097]

The present embodiment is characterized in that high concentration impurity regions suited to respective circuit are made separately in a self-aligned manner or with a mask by the second doping process. The TFT structures of the n-channel TFTs 406, 408, and 409 are all low concentration drain (LDD: Lightly Doped Drain) structures. In addition, the n-channel TFT 406 has a so-called GOLD structure in which the LDD region is disposed overlapping with the gate electrode with the gate insulating film interposed therebetween. In addition, the n-channel TFTs 408 and 409 have structures which only include regions not overlapping with the gate electrodes (LDD regions). Note that low concentration impurity regions ( $n^-$  regions) which overlap with a gate electrode with an insulating film interposed therebetween are referred to as GOLD regions and low concentration impurity regions ( $n^-$  regions) which do not overlap with a gate electrode are referred to as LDD regions in this specification. The width in the channel direction of the regions which do not overlap with a gate electrode (LDD regions) can be freely set by suitably changing the mask used during the second doping process. Furthermore, if the first doping process conditions are changed so that the impurity element is also added below the tapered portions, then it is possible to make the n-channel TFTs 408 and 409 have structures in which regions overlapping with the gate electrodes (GOLD regions) and regions not overlapping with the gate electrodes (LDD regions) are both included.

[0098]

Note that it is possible to apply the method of forming a semiconductor layer of Embodiment mode 2 as a substitute for the method of forming a semiconductor layer of Embodiment mode 1 when forming the semiconductor layers 302 to 306 in the present embodiment.

[0099]

[Embodiment 2]

An example of performing crystallization by a method which differs from that of Embodiment mode 1 is shown in FIG. 6 in the present embodiment.

[0100]

First, a base insulating film 701 and an amorphous semiconductor film 702 are formed on a substrate 700 as Embodiment mode 1. Subsequently, an insulating film containing silicon as its main component is formed and a mask 703 comprising resist is formed. The insulating film is then selectively removed using the mask 703; thus, a mask 704 is formed (FIG. 6A).

[0101]

Next, after removing the mask 703, a metal containing layer 705 is formed. Metal elements are selectively added to the amorphous semiconductor film located in regions not covered with the mask 704 here (FIG. 6B).

[0102]

A heat treatment process is performed next, causing crystallization, and a semiconductor film 706 having a crystalline structure is formed. A heat treatment process using an electric furnace or the irradiation of strong light may be used for the heat treatment process. In the case that the heat treatment using an electric furnace is used, it may be performed at 500 to 650 °C for 4 to 24 hours, for example at 550 °C for 4 hours. Crystallization proceeds along with the diffusion of nickel in directions shown by arrows in FIG. 6C. The amorphous semiconductor film contacting to the mask 704 comprising the insulating film is crystallized due to the action of nickel by the heat treatment process.

[0103]

The mask 704 is removed next, and the semiconductor film 706 having a crystalline structure is obtained. (FIG. 6D)

[0104]

Subsequent processes may be performed in accordance with Embodiment mode 1 or Embodiment 1. Note that FIG. 6D corresponds to FIG. 1B.

[0105]

Further, it is possible to combine the present embodiment with Embodiment mode 2.

[0106]

[Embodiment 3]

In the present embodiment, a process for manufacturing an active matrix liquid crystal display device using the active matrix substrate manufactured in Embodiment 1 will be described. The description is made with reference to FIG. 7.

[0107]

First, after the active matrix substrate with the state of FIG. 5 is obtained according to Embodiment 1, an orientation film is formed on the active matrix substrate of FIG. 5 to perform a rubbing treatment. Note that, in the present embodiment, before forming the orientation film, an organic resin film such as an acrylic resin film is patterned to form a columnar spacer for keeping a gap between substrates in a desired position. In addition, instead of the columnar spacer, a spherical spacer may be distributed over the entire surface of the substrate.



[0108]

Next, an opposing substrate is prepared. A color filter in which a colored layer and a light shielding layer are arranged corresponding to respective pixel is provided in this opposing substrate. In addition, a light shielding layer is also provided in a portion of a driver circuit. A leveling film for covering the color filter and the light shielding layer is provided. Next, an opposing electrode comprising a transparent conductive film is formed in a pixel portion on the leveling film, and then an orientation film is formed on the entire surface of the opposing substrate to perform a rubbing process.

[0109]

Then, the active matrix substrate in which the pixel portion and the driver circuit are formed and the opposing substrate are adhering to each other with a sealing member. The filler is mixed with the sealing member, and two substrates are adhering to each other with a uniform interval by this filler and the columnar spacer. After that, a liquid crystal material is injected into a space between both substrates, and then completely sealed by a sealing agent (not shown). A known liquid crystal material may be used as the liquid crystal material. Thus, the active matrix liquid crystal display device is completed. If necessary, the active matrix substrate or the opposing substrate is cut with a predetermined shape. Also, a polarizing plate and the like are suitably provided using a known technique. And, an FPC is adhering to the active matrix liquid crystal display device by a known technique.

[0110]

A structure of a liquid crystal module thus obtained will be described using a top view of FIG. 7. Note that the same reference numerals are used to portions corresponding to those of FIG. 5.

[0111]

The top view of FIG. 7 shows the state that the active matrix substrate and the opposing substrate 800 are adhering to each other through the sealing member 807. Over the active matrix substrate, a pixel portion, a driver circuit, an external input terminal 809 to which a FPC (Flexible Printed Circuit) 811 is adhering, a wiring 810 for connecting the external input terminal with an input portion of the respective circuits, and the like are formed. Also, the color filter and the like are formed in the opposing substrate 800.

[0112]

A light shielding layer 803a is provided in the opposing substrate side so as to overlap with a gate wiring side driver circuit 401a, and a light shielding layer 803b is

provided in the opposing substrate side so as to overlap with a source wiring side driver circuit 401b. In addition, in a color filter 802 which is provided in the opposing substrate side on a pixel portion 402, a light shielding layer and colored layers for respective colors red color (R), green color (G), and blue color (B) are provided corresponding to respective pixel. Actually, a color display is formed using three colors, that is, the colored layer for the red color (R), the colored layer for the green color (G), and the colored layer for the blue color (B). Note that the colored layers for respective colors are arbitrarily arranged.

[0113]

Here, for a color display, the color filter 802 is provided over the opposing substrate. However, the present invention is not particularly limited to this case, and in manufacturing the active matrix substrate, the color filter may be formed over the active matrix substrate.

[0114]

Also, in the color filter, the light shielding layer is provided between adjacent pixels such that a portion except for a display region is shielded. The light shielding layers 803a and 803b are provided in a region covering the driver circuit. However, when the liquid crystal display device is incorporated into an electronic device as a display portion thereof, the region covering the driver circuit is covered with a cover. Thus, the color filter may be constructed without the light shielding layer. In manufacturing the active matrix substrate, the light shielding layer may be formed over the active matrix substrate.

[0115]

Also, without providing the light shielding layer, the colored layers composing the color filter may be suitably arranged between the opposing substrate and the opposing electrode such that light shielding is made by a lamination layer laminated with a plurality of layers. Thus, the portion except for the display region (gaps between pixel electrodes) and the driver circuit may be shielded.

[0116]

Also, the FPC 811 which is composed of the base film and the wiring is adhering with an anisotropic conductive resin to the external input terminal. Further, a reinforcing plate is provided to increase a mechanical strength.

[0117]

The liquid crystal module manufactured as above can be used as the display portion of various electronic equipments.

[0118]

The above-mentioned liquid crystal module may be either one of AC drive and DC drive.

[0119]

The present embodiment can be freely combined with either one of Embodiment mode 1, Embodiment mode 2, Embodiment 1 and Embodiment 2.

[0120]

[Embodiment 4]

Embodiments 1 or 3 show examples of a reflection type display device in which a pixel electrode is made of reflective metal material. In the present embodiment, an example of a transmission type display device in which a pixel electrode is made of a conductive film having light transparency is shown.

[0121]

The processes before forming an interlayer insulating film 1100 are the same as those in Embodiment 1. Therefore, these processes will be omitted here. After the interlayer insulating film is formed in accordance with Embodiment 1, a pixel electrode 1101 made of a conductive film having light transparency is formed. As the conductive film having light transparency, ITO (indium oxide tin oxide alloy), indium oxide zinc oxide alloy ( $\text{In}_2\text{O}_3\text{-ZnO}$ ), zinc oxide ( $\text{ZnO}$ ), or the like may be used.

[0122]

Thereafter, contact holes are formed in the interlayer insulating film 1100. Then, connection electrodes 1102 overlapping the pixel electrodes 1101 are formed. The connection electrode 1102 is connected to drain regions through the contact holes. Furthermore, a source electrode or a drain electrode of another TFT is also formed simultaneously with the connection electrodes 1102.

[0123]

Herein, an example in which all the driver circuits are formed on a substrate is shown. However, several ICs may be used in part of a driver circuit.

[0124]

An active matrix substrate is formed as described above. A liquid crystal module is manufactured in accordance with Embodiment 3 with the use of the active matrix substrate, then a backlight 1104 and a light guiding plate 1105 are provided and are covered with a cover 1106, whereby an active matrix type liquid crystal display apparatus as shown in FIG. 8 is completed. Note that the cover 1106 and the liquid crystal module are attached to each other with an adhesive or an organic resin. Furthermore, when a substrate is attached to an opposing substrate, the substrate may be bonded to each other by surrounding the substrate with a frame and filling the space

between the frame and the substrate with an organic resin. Since the apparatus is of a transmission type, polarizing plates 1103 are attached to both the active matrix substrate and the opposing substrate.

[0125]

The present embodiment can be combined with either one of Embodiments 1 to 3.

[0126]

[Embodiment 5]

An example of manufacturing a light emitting display device provided with EL (Electro Luminescence) elements is shown in FIG. 9 in the present embodiment.

[0127]

FIG. 9A is a top view showing an EL module, and FIG. 9B is a cross sectional view of FIG. 9A cut along a line A-A'. A pixel portion 902, a source side driver circuit 901, and a gate side driver circuit 903 are formed on a substrate 900 having an insulating surface (for example a glass substrate, a crystallized glass substrate, or a plastic substrate). The pixel portion and the driver circuits can be obtained in accordance with the above-mentioned embodiments. Further, reference numeral 918 denotes a sealing material, and reference numeral 919 denotes a DLC film. The pixel portion and the driver circuit portions are covered with the sealing material 918, and the sealing material is covered with a protective film 919. In addition, sealing is performed by a cover material 920 using an adhesive. It is preferable that the cover material 920 be the same substance as the substrate 900 in order to be able to withstand changes in shape due to heat and external forces, for example a glass substrate, and a concave shape (depth 3 to 10  $\mu\text{m}$ ) is produced as shown in FIG.9 by a method such as sand blasting. In addition, it is preferable to form a concave portion (depth 50 to 200  $\mu\text{m}$ ) in which it is possible to place a drying agent 921. Furthermore, if multiple EL modules are manufactured from one substrate, then after joining the substrate and the cover material, sectioning may be performed using means such as a CO<sub>2</sub> laser, so that end faces become uniform.

[0128]

Note that reference numeral 908 denotes a wiring for transmitting input signals inputted to the source side driver circuit 901 and the gate side driver circuit 903. Video signals and clock signals are received from an FPC (flexible printed circuit) 909 to be an external input terminal. Note that although only the FPC is shown in the figures here, a printed wiring board (PWB) may also be attached to the FPC. The light emitting device in this specification includes not only the light emitting device itself,

but also a state in which an FPC or a PWB are attached thereto.

[0129]

The cross sectional structure is explained next using FIG. 9B. An insulating film 910 is formed on the substrate 900, and the pixel portion 902 and the gate side driver circuit 903 are formed on the upper side of the insulating film 910. The pixel portion 902 is formed by a plurality of pixels containing an electric current control TFT 711 and a pixel electrode 912 that is electrically connected to the drain of the electric current control TFT 711. Further, the gate side driver circuit 903 is formed using a CMOS circuit in which an n-channel TFT 913 and a p-channel TFT 914 are combined.

[0130]

The TFT (including 911, 913, and 914) may be manufactured in accordance with above Embodiment 1.

[0131]

The pixel electrode 912 functions as an anode of an EL element. Further, banks 915 are formed at both edges of the pixel electrode 912, and an EL layer 916 and a cathode of an EL element 917 are formed on the pixel electrode 912.

[0132]

As the EL layer 916, an EL layer (a layer for emitting light and for carrier mobility in order to emit light) may be formed by freely combining a light emitting layer, a charge transport layer, or a charge injection layer. For example, low molecular weight organic EL materials or high molecular weight organic EL materials may be used. Furthermore, a thin film comprising a light emitting material (singlet compound) that emits light by singlet excitation (fluorescence), or a thin film comprising a light emitting material (triplet compound) that emits light by triplet excitation (phosphorescence) can be used as an EL layer. It is also possible to use inorganic materials such as silicon carbide, as a charge transport layer or a charge injection layer. Known materials can be used for these organic EL materials and inorganic materials.

[0133]

The cathode 917 functions as a common wiring for all pixels, and is electrically connected to the FPC 909 via a connection wiring 908. In addition, elements contained in the pixel portion 902 and the gate side driver circuit 903 are all covered with the cathode 917, the sealing material 918, and the protective film 919.

[0134]

Note that it is preferable to use a material which is as transparent or semi-transparent as possible with respect to visible light, as the sealing material 918.

Further, it is also preferable that the sealing material 918 be a material which does not let moisture and oxygen go through as much as possible.

[0135]

It is also preferable that, after the light emitting element is completely covered with the sealing material 918, the protective film 919 made of a DLC film or the like is formed on the surface (exposed surface) of the sealing material 918 as shown in FIG. 9 at least. The protective film may also be formed over the entire surface of the substrate, including the back surface. It is necessary to take care here such that the protective film is not formed in portions at which the external input terminal (FPC) is provided. A mask may be used so that the protection film is not formed, or a tape such as Teflon used as a masking tape in a CVD apparatus may cover the portion of the external input terminal so that the protection film is not formed.

[0136]

The EL elements can be completely shut off from the outside by thus enclosing the EL elements with the sealing material 918 and the protective film, whereby the incursion of substances such as moisture and oxygen from the outside which promote deterioration of the EL layer by inducing oxidation thereof can be prevented. Therefore, a light emitting device having high reliability can be obtained.

[0137]

By forming the pixel electrode as the cathode and stacking the EL layer and the anode, a structure in which light is emitted in a direction opposite to that of FIG. 9 may also be used. One example of such a structure is shown in FIG. 10. Note that a top view is identical to that of FIG. 9A and is therefore omitted.

[0138]

The cross sectional structure shown in FIG. 10 is explained below. In addition to a glass substrate or a quartz substrate, a semiconductor substrate or a metal substrate can also be used as a substrate 1000. An insulating film 1010 is formed on the substrate 1000, and a pixel portion 1002 and a gate side driver circuit 1003 are formed on the upper side of the insulating film 1010. The pixel portion 1002 is composed of a plurality of pixels including an electric current control TFT 1011 and a pixel electrode 1012 which is electrically connected to a drain of the electric current control TFT 1011. The gate side driver circuit 1003 is formed using a CMOS circuit in which an n-channel TFT 1013 and a p-channel TFT 1014 are combined.

[0139]

The pixel electrode 1012 functions as a cathode of the EL element. Further, banks 1015 are formed at both edges of the pixel electrode 1012, and an EL layer 1016

and an anode of an EL element 1017 are formed on the pixel electrode 1012.

[0140]

The anode 1017 functions as a common wiring for all pixels, and is electrically connected to an FPC 1009 via a connection wiring 1008. In addition, elements contained in the pixel portion 1002 and the gate side driver circuit 1003 are all covered with the anode 1017, sealing material 1018, and a protective film 1019 comprising DLC and the like. The covering material 1021 and the substrate 1000 are joined by an adhesive. Further, a concave portion is formed in the covering material, and a drying agent 1021 is disposed.

[0141]

Note that it is preferable to use a material which is as transparent or semi-transparent as possible with respect to visible light, as the sealing material 1018. Further, it is also preferable that the sealing material 1018 be a material which does not let moisture and oxygen go through as much as possible.

[0142]

The pixel electrode is used as the cathode, and the EL layer and the anode are laminated in FIG. 10. Thus, the direction of light emitted becomes the direction of the arrow shown in FIG. 10.

[0143]

Note that it is possible to combine the present embodiment with any one of Embodiments 1 to 4.

[0144]

[Embodiment 6]

The present embodiment shows an example different from Embodiment 1 with reference to FIG. 11.

[0145]

First, a conductive film is formed on a substrate 11 having an insulating surface and is patterned, whereby scanning lines 12 are formed. The scanning lines 12 function as shading layers for protecting an active layer formed later from light. Herein, a quartz substrate is used as the substrate 11, and a layered structure of a poly-silicon film (thickness: 50 nm) and a tungsten silicide (W-Si) film (thickness: 100 nm) are used as the scanning lines 12. The poly-silicon film protects the substrate from contamination due to tungsten silicide.

[0146]

Then, insulating films 13a and 13b covering the scanning lines 12 are formed to a thickness of 100 to 1000 nm (typically, 300 to 500 nm). Herein, a silicon oxide

film (thickness: 100 nm) formed by CVD and a silicon oxide film (thickness: 280 nm) formed by LPCVD are stacked.

[0147]

An amorphous semiconductor film is formed to a thickness of 10 to 100 nm. Herein, an amorphous silicon film (thickness: 69 nm) are formed by LPCVD. Then, crystallization, gettering, and patterning are conducted using the technique described in Embodiment modes 1 or 2 as a technique of crystallizing the amorphous semiconductor film to remove unnecessary portions of a crystalline silicon film, whereby a semiconductor layer 14 is formed.

[0148]

Then, in order to form a storage capacitor, a mask is formed, and a part (region where a storage capacitor is to be formed) of the semiconductor layer is doped with phosphorus.

[0149]

Then, the mask is removed, and an insulating film covering the semiconductor layer is formed. Thereafter, a mask is formed, and the insulating film on the region where a storage capacitor is to be formed is selectively removed.

[0150]

The mask is removed and thermal oxidation is conducted, whereby an insulating film (gate insulating film) 15 is formed. Due to the thermal oxidation, the final thickness of the gate insulating film becomes 80 nm. Note that on the region where a storage capacitor is to be formed, an insulating film which is thinner than that of the other region is formed.

[0151]

Then, channel dope step to add a p-type or n-type impurity element in a low concentration to regions to be channel regions of TFTs is conducted either to the entire surface or selectively. The channel dope step is the one that controls a threshold voltage of TFTs. Herein, boron is added by ion doping in which diborane ( $B_2H_6$ ) is excited with plasma without mass segregation. Needless to say, ion implantation in which mass segregation is conducted may be used.

[0152]

Next, a mask is formed on the insulating film 15, and the insulating films 13a and 13b, and then a contact hole reaching the scanning line 12 is formed. After formation of the contact hole, the mask is removed.

[0153]

A conductive film is formed and is patterned, whereby gate electrodes 16 and a



capacitor wiring 17 are formed. Herein, a layered structure of a silicon film (thickness: 150 nm) doped with phosphorus and tungsten silicide (thickness: 150 nm) is used. The storage capacitor is composed of the insulating film 15 as a dielectric, the capacitive wiring 17, and part of the semiconductor layer.

[0154]

Phosphorus is added in a low concentration in a self-alignment manner, using the gate electrodes 16 and the capacitive wiring 17 as a mask. The concentration of phosphorus in regions where phosphorus is added in a low concentration is regulated to be  $1 \times 10^{16}$  to  $5 \times 10^{18}$  atoms/cm<sup>3</sup>, typically  $3 \times 10^{17}$  to  $3 \times 10^{18}$  atoms/cm<sup>3</sup>.

[0155]

Then, a mask is formed and phosphorus is added in a high concentration, whereby high concentration impurity regions to be a source region or a drain region are formed. The concentration of phosphorus in the high concentration impurity regions is regulated to  $1 \times 10^{20}$  to  $1 \times 10^{21}$  atoms/cm<sup>3</sup> (typically,  $3 \times 10^{19}$  to  $3 \times 10^{20}$ /cm<sup>3</sup>). In the semiconductor layer 14, regions overlapping the gate electrodes 16 become channel formation regions, and regions covered with the mask become low concentration impurity regions that function as LDD regions. After addition of the impurity element, the mask is removed.

[0156]

Then, in order to form a p-channel TFT used in a driver circuit formed on the same substrate as that of pixels, a region to be an n-channel TFT is covered with a mask, and boron is added to form a source region or a drain region.

[0157]

After a mask 412 is removed, a passivation film 18 covering the gate electrodes 16 and the capacitive wiring 17 is formed. Herein, a silicon oxide film is formed to a thickness of 70 nm. Then, the n-type or p-type impurity elements added in the respective concentrations in the semiconductor layer are activated by heat treatment or irradiation with strong light. Herein, activation is conducted by irradiation with a YAG laser from the back surface. An excimer laser may be used, in place of a YAG laser.

[0158]

Then, an interlayer insulating film 19 comprising an organic resin material is formed. Herein, an acrylic resin film having a film thickness of 400 nm is used. Then, after a contact hole reaching the semiconductor layer is formed, an electrode 20 and a source wiring 21 are formed. In the present embodiment, the electrode 20 and the source wiring 21 were composed of a three layered structure formed by continuously forming a Ti film (thickness: 100 nm), an aluminum film containing Ti

(thickness: 300 nm), and a Ti film (thickness: 150 nm) by sputtering.

[0159]

After hydrogenation is conducted, an interlayer insulating film 22 comprising acrylic is formed. Then, a conductive film (thickness: 100 nm) having light transparency is formed on the interlayer insulating film 22, whereby a light shielding layer 23 is formed. Then, an interlayer insulating film 24 is formed. A contact hole reaching the electrode 20 is formed. Then, after a transparent conductive film (herein, indium tin oxide (ITO) film) having a thickness of 100 nm is formed, it is patterned to obtain a pixel electrode 25.

[0160]

Needless to say that the present embodiment is one example and the present invention is not limited to the processes of the present embodiment. For example, as each conductive film, an element selected from tantalum (Ta), titanium (Ti), molybdenum (Mo), tungsten (W), chromium (Cr), and silicon (Si), or an alloy film (typically a Mo-W alloy, a Mo-Ta alloy) obtained by combining the elements can be used. Furthermore, as each insulating film, a silicon oxide film, a silicon nitride film, a silicon oxynitride film, and a film comprising an organic resin material (polyimide, acrylic, polyamide, polyimideamide, BCB (benzocyclobutene) or the like) can be used.

[0161]

The present embodiment can be combined with either one of Embodiments 1 to 5.

[0162]

[Embodiment 7]

In Embodiment 1, a top gate type TFT has been explained. The present invention is also applicable to a bottom gate type TFT shown in FIG. 12.

[0163]

FIG. 12A is a top view showing an enlarged pixel in a pixel portion. In FIG. 12A, a portion cut along a dotted line A-A' corresponds to a cross-sectional structure of the pixel portion in FIG. 12B.

[0164]

In the pixel portion shown in FIG. 12, a pixel TFT portion is composed of an n-channel TFT. Gate electrodes 52 are formed on a substrate 51, and a first insulating film 53a comprising silicon nitride and a second insulating film 53b comprising silicon oxide are provided thereover. On the second insulating film, source regions or drain regions 54 to 56 as an active layer, channel formation regions 57 and 58, and LDD regions 59 and 60 between the source region or drain region and the channel formation

region are formed. The channel formation regions 57 and 58 are protected with insulating layers 61 and 62. After contact holes are formed in the first interlayer insulating film 63 covering the insulating layers 61, 62 and the active layer, a wiring 64 connected to the source region 54 and a wiring 65 connected to the drain region 56 are formed and a passivation film 66 is further formed thereover. Then, a second interlayer insulating film 67 is formed thereover. Furthermore, a third interlayer insulating film 68 is formed thereover. A pixel electrode 69 comprising a transparent conductive film such as ITO and  $\text{SnO}_2$  is connected to the wiring 65. Reference numeral 70 denotes a pixel electrode adjacent to the pixel electrode 69.

[0165]

In the present embodiment, an active layer is formed in accordance with above Embodiment modes 1 or 2.

[0166]

In the present embodiment, a bottom gate type TFT of channel stop type has been described as an example. However, the present invention is not particularly limited thereto.

[0167]

Note that in the present embodiment, a gate wiring of a pixel TFT in the pixel portion has a double gate structure. However, in order to reduce variation in an OFF current, a multi gate structure such as a triple gate structure may be used. Further, in order to enhance an aperture ratio, a single gate structure may be used.

[0168]

In addition, a capacitor part of the pixel portion is composed of a first and a second insulating film as a dielectric, a capacitor wiring 71, and the drain region 56.

[0169]

Note that the pixel portion shown in FIG. 12 is an example, and the pixel portion is not particularly limited to the above-mentioned configuration.

[0170]

The present embodiment can be combined with either one of Embodiments 1 to 4.

[0171]

[Embodiment 8]

The driver circuit and the pixel portion fabricated by implementing the present invention can be utilized for various modules (active matrix liquid crystal module, active matrix EL module and active matrix EC module). In other words, all of the electronic apparatuses which incorporated them in a display portion can embody the

present invention.

[0172]

Such an electronic apparatus include a video camera, a digital camera, a head mounted display (a goggle type display), a car navigation system, a projector, a car stereo, a personal computer, a portable information terminal (such as a mobile computer, a mobile phone or an electronic book) and the like. Examples of these are shown in FIGS. 13 to 15.

[0173]

FIG. 13A is a personal computer which comprises a main body 2001, an image input portion 2002, a display portion 2003, and a key board 2004 and the like. The present invention can be applied to the display portion 2003.

[0174]

FIG. 13B is a video camera which comprises a main body 2101, a display portion 2102, a voice input portion 2103, operation switches 2104, a battery 2105 and an image receiving portion 2106 and the like. The present invention can be applied to the display portion 2102.

[0175]

FIG. 13C is a mobile computer which comprises a main body 2201, a camera portion 2202, an image receiving portion 2203, operation switches 2204 and a display portion 2205 and the like. The present invention can be applied to the display portion 2205.

[0176]

FIG. 13D is a goggle type display which comprises a main body 2301, a display portion 2302 and an arm part 2303 and the like. The present invention can be applied to the display portion 2302.

[0177]

FIG. 13E is a player using a recording medium in which a program is recorded (hereinafter referred to as a recording medium), comprising a main body 2401, a display portion 2402, a speaker portion 2403, a recording medium 2404, and an operation switch 2405 and the like. This apparatus uses DVD (Digital Versatile Disc), CD, and the like for the recording medium, and can perform music appreciation, movie appreciation, games and use for Internet. The present invention can be applied to the display portion 2402.

[0178]

FIG. 13F is a digital camera which comprises a main body 2501, a display portion 2502, an eye piece portion 2503, operation switches 2504 and an image

receiving portion (not shown in the figure) and the like. The present invention can be applied to the display portion 2502.

[0179]

FIG. 14A is a front type projector which comprises a projection device 2601 and a screen 2602 and the like. The present invention can be applied to the liquid crystal module 2808 which configures a part of the projection device 2601.

[0180]

FIG. 14B is a rear type projector which comprises a main body 2701, a projection device 2702, a mirror 2703 and a screen 2704 and the like. The present invention can be applied to the liquid crystal module 2808 which configures a part of the projection device 2702.

[0181]

FIG. 14C is a diagram which shows an example of the structure of a projection device 2601 and 2702 in FIGS. 14A and 14B. Each of the projection devices 2601 and 2702 comprises a light source optical system 2801, mirrors 2802 and 2804 to 2806, a dichroic mirror 2803, a prism 2807, a liquid crystal module 2808, phase differentiating plates 2809 and projection optical system 2810. The projection optical system 2810 comprises an optical system having a projection lens. The present embodiment shows an example of a three-plate type, however it is not limit to the present embodiment and a single-plate type may be used for instance. Further, a dispenser may appropriately dispose an optical lens, a film which has a function to polarize light, a film which adjusts a phase difference, an IR film or the like in the optical path shown by an arrow in FIG. 14C.

[0182]

FIG. 14D is a diagram showing an example of a structure of a light source optical system 2801 in FIG. 14C. In the present embodiment the light source optical system 2801 comprises a reflector 2811, a light source 2812, lens arrays 2813 and 2814, a polarizer conversion element 2815 and a condenser lens 2816. Note that the light source optical system shown in FIG. 14D is merely an example and the structure is not particularly limited thereto. For example, a dispenser may appropriately dispose optical systems such as an optical lens, a film which has a function to polarize light, a film which adjusts a phase difference, an IR film.

[0183]

However, the projectors shown in FIG. 14 are the cases of using a transmission type electro-optical devices, and applicable examples of a reflection type electro-optical device and an EL module are not shown.

[0184]

FIG. 15A is a mobile phone which comprises a main body 2901, a voice output portion 2902, a voice input portion 2903, a display portion 2904, operation switches 2905, an antenna 2906, an image input portion (for example, CCD and image sensor) 2907 and the like. The present invention can be applied to the display portion 2904.

[0185]

FIG. 15B is a portable book (electronic book) which comprises a main body 3001, display portions 3002 and 3003, a recording medium 3004, operation switches 3005, an antenna 3006 and the like. The present invention can be applied to the display portions 3002 and 3003.

[0186]

FIG. 15C is a display which comprises a main body 3101, a support 3102, a display portion 3103 and the like. The present invention can be applied to the display portion 3103.

[0187]

As described above, the applicable range of the present invention is very large, and the invention can be applied to manufacturing methods of electronic apparatuses of various areas. In addition, the electronic devices of the present embodiment can be achieved by utilizing any combination of constitutions in Embodiments 1 to 7.

[0188]

[Effect of the Invention]

According to the present invention, the number of high temperature (equal to or greater than 600 °C) heat treatment process steps can be reduced and lower temperature (equal to or less than 600 °C) processes can be realized. In addition, simplification of a step and improvement of throughput can be realized.

[0189]

Furthermore, in the case that a rare gas element is added, a rare gas element in a high concentration can be added in a short time about 1 or 2 minutes to a semiconductor film. Therefore the throughput can be improved remarkably compared to gettering using phosphorous.

[0190]

Further, a gettering ability of the present invention using a rare gas element is high compared to gettering using phosphorous, and a rare gas element can be added in further a high concentration, for example from  $1 \times 10^{20}$  to  $5 \times 10^{21} / \text{cm}^3$ . Therefore the amount of a metal element added for use in crystallization can be increased. In other words, it becomes possible to perform crystallization processing at a shorter processing

time by increasing the addition amount of the metal element used in the crystallization. Furthermore, even if the length of crystallization processing time is not changed, crystallization can be performed at a lower temperature by increasing the addition amount of the metal element used in the crystallization. In addition, spontaneous nucleation can be reduced, and a semiconductor film having a good crystallinity can be formed by increasing the addition amount of the metal element used in the crystallization.

[Brief Description of the Drawings]

[FIG. 1] is a diagram showing a process of manufacturing a TFT.

[FIG. 2] is a diagram showing a process of manufacturing a TFT.

[FIG. 3] is a diagram showing a process of manufacturing an active matrix substrate.

[FIG. 4] is a diagram showing a process of manufacturing an active matrix substrate.

[FIG. 5] is a diagram showing a process of manufacturing an active matrix substrate.

[FIG. 6] is a diagram showing crystallization of a semiconductor film.

[FIG. 7] is a top view of an active matrix liquid crystal display device.

[FIG. 8] is a diagram showing a transmission type example.

[FIG. 9] is a top view and a cross sectional view showing an EL module.

[FIG. 10] is a cross sectional view showing an EL module.

[FIG. 11] is a cross sectional view of an active matrix substrate.

[FIG. 12] is a cross sectional view and a top view of an active matrix substrate.

[FIG. 13] is a diagram showing examples of electronic equipment.

[FIG. 14] is a diagram showing examples of electronic equipment.

[FIG. 15] is a diagram showing examples of electronic equipment.

[FIG. 16] is a graph showing a relationship between argon gas flow rate and an internal stress of a film.

[Name of Document]      Abstract

[Abstract]

[Object]

It is an object to reduce the number of high temperature (equal to or greater than 600 °C) heat treatment processes and achieve lower temperature (equal to or less than 600 °C) processes, and to simplify the process steps and improve throughput.

[Means for solving]

In the present invention, a barrier layer 105, a second semiconductor film 106, and a third semiconductor film 108 containing a rare gas element are formed on a first semiconductor film 104 having a crystalline structure. After gettering in which a metal element contained in the first semiconductor film 104 passes through the barrier layer 105 and the second semiconductor film 106 by a heat treatment process, and moves to the third semiconductor film 108 is performed, the second semiconductor film 106 and the third semiconductor film 108 are removed with the barrier layer 105 used as an etching stopper.

[Selected drawing]      FIG. 1